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09/685,192	10/11/2000	Anders Johnson	108339-00031	5268

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EXAMINER

HA, LEYNNA A

ART UNIT PAPER NUMBER

2135

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/685,192

Applicant(s)

JOHNSON, ANDERS

Examiner

LEYNNA T. HA

Art Unit

2135

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 28 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-4, 7-9, 12-17, 19-23, AND 27-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4, 7-9 and 12 is/are allowed.
- 6) ☒ Claim(s) 13-17, 19-23 and 27-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. Claims 1-4, 7-9, 12-17, 19-23, and 27-29 are pending.

Applicant have amended claim 1.

Applicant have cancelled claims 5-6, 10-11, 18, and 24-26.

2. Claims 1-4, 7-9, and 12 are allowed over art.

Claims 13-17, 19-23, and 27-29 remains rejected.

***Continued Examination Under 37 CFR 1.114***

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 28, 2005 has been entered.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**4. Claims 13-17, 19-23, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tello (US 6,463,537) and further view in view of Angelo, et al. (US 6,370,649).**

**As per claim 13:**

Tello discloses a component for selectively enabling functionality of an electronic device comprising a means for generating an encrypted bit string (COL.15, lines 7-11), a hash function module in communication with the identification module (COL.15, lines 21-23) and a means for acquiring a guess passcode (COL.9, lines 20-24). Tello includes a hash function in communication with an on board memory having a predefined identification number stored therein (COL.9, lines 26-30) and means for determining if the encrypted bit string matches the guess passcode (COL.16, lines 40-55 and COL.24, lines 47-52) and means for outputting a functionality enable signal (col.19, lines 12-25 and col.37, lines 27-42). Tello teach a selecting device as the control line (PIDEMIST\_CTRL) is used to disable or enable the Primary Master IDE slot. The PIDEMIST\_CTRL logically connects to the programmable device which is

connected to the security engine microprocessor and the OR gate which is connected to the AND gate which in turn is connected through a Slave line to the data switch IC (COL.13, lines 15-17) and connected to the control line between the OR gate which is connected to the AND gate and the programmable device is the pull up resistor (COL.13, lines 56-58) of which the switch and the pull up resistor makes the bonding option output. Therefore, Tello has the capability to set the control line to HIGH or LOW wherein having the selecting device to either disable the line or enable the line to allow the motherboard microprocessor to recognize a device connected to the Primary Slave IDE slot (COL.13, lines 59-67) that comprises an OR gate having at least one input for receiving the function enable output and the bonding option output.

However, Tello fails to include the acquiring the passcode or password from a manufacturer.

Angelo teaches a computer system that implements a fail safe password system that allows the manufacturer to securely supply a password to users (col.2, lines 1-2) that is based on the date and serial number (col.6, lines 16-18). It would have been obvious for a person of ordinary skills in the art to communicate to request a password corresponding to the identification number because the password supplied by the manufacturer is stored in a secure non-volatile memory that helps ensure users who lose or misplace their passwords from being bypassed and by the manufacturer supplying the password is less likely to obtain than if the passwords were to be stored in the computers themselves (col.1, lines 31-63).

**As per claim 14:** See Tello on col.20, lines 1-23 discussing the a public key encryption module is in communication with the public key module having a public key stored therein and a guess register in communication (col.19, lines 12-25 and col.37, lines 27-42) with the public key encryption module wherein receives the guess passcode from the guess register and the public key from the public key module in order to generate a ciphertext bit string (COL.37, line 26 – COL.38, line 7).

**As per claim 15:**

Tello discloses a host in communication with means for generating an encrypted bit string (COL.15, lines 7-11), an identification module in communication with the host (COL.9, lines 20-24) wherein the host is configured to communicate (col.19, lines 12-25 and col.37, lines 27-42) with a manufacturer of the component to request the guess passcode corresponding to an identification number stored in the identification module (COL.38, lines 11-48).

**As per claim 16:**

Tello includes an onboard nonvolatile register having an identification number stored therein (col.14, lines 62-63 and col.24, lines 46-52) and a one-way hash function module that receives an identification number from the on board memory and generates a corresponding hash value (col.16, lines 30-33).

**As per claim 17:** See Tello on col.24, lines 48-52 discussing a comparator.

**As per claim 18:** Cancelled

**As per claim 19:** See Tello on col.11, lines 50-52 discussing the network switch and a media access controller.

**As per claim 20:**

Tello discloses the steps of encrypting a first bit string and a second bit string to generate a third bit string (COL.37, line 26 – COL.38, line 7), calculating the fourth bit string (COL.16, lines 30-33), comparing the fourth bit string to the third bit string, and generating the function enable signal in accordance with the comparison (col.15, lines 52-65 and col.16, lines 13-26). Tello teaches a selecting device as the control line (PIDEMIST\_CTRL) is used to disable or enable the Primary Master IDE slot. The PIDEMIST\_CTRL logically connects to the programmable device which is connected to the security engine microprocessor and the OR gate which is connected to the AND gate which in turn is connected through a Slave line to the data switch IC (COL.13, lines 15-17) and connected to the control line between the OR gate which is connected to the AND gate and the programmable device is the pull up resistor (COL.13, lines 56-58) of which the switch and the pull up resistor makes the bonding option output. Therefore, Tello has the capability to set the control line to HIGH or LOW wherein having the selecting device to either disable the line or enable the line to allow the motherboard microprocessor to recognize a device connected to the Primary Slave IDE slot (COL.13, lines 59-67) that comprises an OR gate having at least one input for receiving the function enable output and the bonding option output.

However, Tello fails to include determining the password by requesting a password from a manufacturer.

Angelo teaches a computer system that implements a fail safe password system that allows the manufacturer to securely supply a password to users (col.2, lines 1-2)

that is based on the date and serial number (col.6, lines 16-18). It would have been obvious for a person of ordinary skills in the art to communicate to request a password corresponding to the identification number because the password supplied by the manufacturer is stored in a secure non-volatile memory that helps ensure users who lose or misplace their passwords from being bypassed and by the manufacturer supplying the password is less likely to obtain than if the passwords were to be stored in the computers themselves (col.1, lines 31-63).

**As per claim 21:** See Tello on col.20, lines 1-23 discusses receiving the public key and a guess passcode in an encryption module wherein encrypting the public key and the passcode to generate a ciphertext bit string (COL.37, line 26 – COL.38, line 7).

**As per claim 22:** See Tello on col.16, lines 30-32 discussing generating a hash value corresponding to the hash function module.

**As per claim 23:**

Tello discusses the fourth bit string representing the hash value (COL.16, lines30-33) and the third bit string representing the ciphertext bit string (COL.37, line 26 – COL.38, line 7) and comparing the fourth bit string to the third bit string (col.15, lines 52-65 and col.16, lines 13-26).

**As per claim 24:** Cancelled

**As per claim 25:** Cancelled

**As per claim 26:** Cancelled



**As per claim 27:** See Tello on col.9, lines 21-31 and col.24, lines 15-23; discusses calculating the passcode with the predetermined algorithm and transmitting the passcode to an on board host.

**As per claim 28:** See Tello on col.20, lines 13-15 discussing the different types of connections.

**As per claim 29:** See Tello on col.11, lines 50-52 discussing the network switch and a media access controller.

### ***Response to Arguments***

#### **4. Applicant's arguments are not persuasive.**

Applicant have amended independent claim 1 with new limitations that makes claims 1-4, 7-9 and 12 in condition for allowance. However, claims 13-17, 19-23, and 27-29 did not include the allowable limitation, thus, remains rejected because prior art Tello still reads on the claimed invention as previously presented.

Tello teach a selecting device as the control line (PIDEMIST\_CTRL) is used to disable or enable the Primary Master IDE slot. The PIDEMIST\_CTRL logically connects to the programmable device which is connected to the security engine microprocessor and the OR gate which is connected to the AND gate which in turn is connected through a Slave line to the data switch IC (COL.13, lines 15-17) and connected to the control line between the OR gate which is connected to the AND gate and the programmable device is the pull up resistor (COL.13, lines 56-58) of which the switch and the pull up

resistor makes the bonding option output. Therefore, Tello has the capability to set the control line to HIGH or LOW wherein having the selecting device to either disable the line or enable the line to allow the motherboard microprocessor to recognize a device connected to the Primary Slave IDE slot (COL.13, lines 59-67) that comprises an OR gate for receiving the function enable output and the bonding option output.

The Examiner finds that the OR gate is inherently known for controlling access to privileged functions and to switch tasks. Hence, Tello discloses a selecting device that comprises the OR gate having at least one input for receiving functions such as the function enable output and the bonding option output.

To clarify the inherent functions of the OR gate, the Examiner points to the Microsoft Computer Dictionary. According to the Microsoft Computer Dictionary, a gate is an electronic switch that produces an electrical output signal that represent a binary 1 or 0 and is released to the states of one or more input signals by an operation of Boolean logic and is a data structure used to control access to privileged functions, to change data segments, or to switch tasks (pg.232). The term, "OR gate" is defined as one of the three basic logic gates from which all digital systems can be built and the output of an OR circuit is true (1) if any input is true (pg.381). Therefore, it is inherent the selecting device comprises the OR gate is used to control access to privileged functions, to change data segments, or to switch tasks. Thus, the selecting device of Tello can disable or enable the line to allow the motherboard microprocessor to recognize the device connected to the Primary Slave IDE slot because of the OR gate which controls access to privileged functions and able to switch tasks.

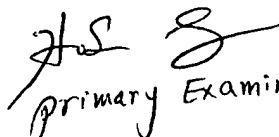
**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEYNNA T. HA whose telephone number is (571) 272-3851. The examiner can normally be reached on Monday - Thursday (7:00 - 5:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LHa

  
Primary Examiner  
Art Unit 2135